AMENDED CLAIM SET

Claim 1. (Currently Amended)

A non-volatile passive matrix memory device comprising;

an electrically polarizable dielectric memory material exhibiting hysteresis, particularly a ferroelectric material, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes, wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device, wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, where each memory cell is at all times in ohmic contact with a word line and a bit line, wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage larger than the coercive voltage Vc, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment

is connected with ~~an~~ a different associated sensing means, such that the word line of the same position within each segment is sensed at the associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 2. (Previously Presented)

A non-volatile passive matrix memory device according to claim 1, wherein simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Claim 3. (Previously Presented)

A non-volatile passive matrix memory device according to claim 2, wherein the number of multiplexers corresponds to the largest number of bit lines defining a segment, each bit line of a segment being connected with a specific multiplexer.

Claim 4. (Previously Presented)

A non-volatile passive matrix memory device according to claim 3, wherein the output of each multiplexer is connected with a single sensing means.

Claim 5. (Previously Presented)

A non-volatile passive matrix memory device according to claim 4, wherein the single sensing means is a sense amplifier.

Claim 6. (Previously Presented)

A non-volatile passive matrix memory device according to claim 1, wherein simultaneous connection of each bit line of a segment to an associated sensing means during addressing is accomplished by a gate means.

Claim 7. (Previously Presented)

A non-volatile passive matrix memory device according to claim 6, wherein all bit lines of a segment are connected with a specific gate means, each gate means having a number of outputs corresponding to the number of bit lines in the respective segment, that each output of each gate means is connected with a specific bus line of an output data bus, the number of bus lines thus corresponding to largest number of bit lines in a segment, and that each bus line is connected with a single sensing means.

Claim 8. (Previously Presented)

A non-volatile passive matrix memory device according to claim 6, wherein the gate means comprise pass gates.

Claim 9. (Previously Presented)

A non-volatile passive matrix memory device according to claim 6, wherein the sensing means is a sense amplifier.

Claim 10. (Withdrawn)

A method for readout of a non-volatile passive matrix memory device (10) comprising an electrically polarizable dielectric memory material (12) exhibiting hysteresis, particularly a ferroelectric material, wherein said memory material (12) is provided sandwiched in a layer between a first set and second set (14;15) of respective parallel addressing electrodes, wherein the electrodes of the first set (14) constitute word lines (WL) of the memory device (10) and are provided in substantially orthogonal relationship to the electrodes of the second set (15), the latter constituting bit lines (BL1,...n) of the memory device (l0), wherein a memory cell (13) with a capacitor-like structure is defined in the memory material (12) at crossings between word lines (WL) and bit lines (BL), wherein the memory cells (13) of the memory device (10) constitute the elements of a passive matrix (11), wherein each memory cell (13) can be selectively addressed for a write/read operation via a word line (WL) and bit line (BL), wherein write operation to a memory cell (13) takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line (WL) and bit line (BL) defining the cell, said applied voltage either establishing a determined polarization state in the cell or being able to switch the cell between the polarization states thereof, wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage Vs to the memory cell (13) and detecting at least one electrical parameter of an output current on its bit lines (BL), and wherein the method comprises steps for controlling electric potentials on all word lines (WL)

and bit lines (BL) in a time-coordinated fashion according to a protocol comprising electric timing sequences for all word lines and bit lines, arranging said protocol to comprise a read cycle, and providing during the read cycle for the sensing means to sense charges flowing in the bit lines, and wherein the method is characterized by dividing the word lines (WL) into a number of segments (S1,...Sq), each segment comprising and being defined by a number of adjacent bit lines (BL) in the matrix (11), connecting each bit line (BL) within a word line segment (S) with an associated sensing means (26), activating according to the protocol one word line (WL) of a segment (S) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage Vs, during at least a portion of the read cycle, while keeping all bit lines of the segment (S) at zero potential, and determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

Claim 11. (Withdrawn)

Method for readout according to claim 10, characterized by keeping all word lines (WL) and bit lines (BL) when no memory cell (13) is read or written, at a quiescent voltage of approximately □ of the switching voltage Vs, activating according to the protocol one word line (WL) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage Vs, during at least a portion of the read cycle, while keeping all bit lines (BL) of the segment (S) at zero potential, and

determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

Claim 12. (Currently Amendment)

A volumetric data storage apparatus comprising:

a plurality of stacked layers, each layer including one non-volatile passive matrix memory device, the non-volatile passive matrix memory device including an electrically polarizable dielectric memory material exhibiting hysteresis, particularly a ferroelectric material,

wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes,

wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines,

wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line and where each memory cell is at all times in ohmic contact with a word line and a bit line, wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell,

wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage Vs, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with ~~an~~ a different associated sensing means, such that the word line of the same position within each segment is sensed at the associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 13. (Currently Amended)

A memory device, comprising:

a first set of electrodes which constitute word lines of the memory device;

a second set of electrodes which constitute bit lines of the memory device, the second set of electrodes being positioned substantially orthogonal to the first set of electrodes, the bit lines being divided into a number of segments;

an electrically polarizable dielectric memory material provided in a layer between the first and second set of electrodes, the electrically polarizable dielectric memory material and the first and second set of electrodes forming a passive matrix memory in which each memory cell can be selectively addressed for a write/read operation and where the memory material is at all times in ohmic contact with the first and second set of electrodes; and

a number of sensing devices connected to each of a corresponding bit lines within each segment of word lines, where each word line in each segment is differentiated based on the position of the word line within the segment, each word line of each segment being adjoined to a separate bit line, such that the word line of the same position within each segment is sensed at an associated sensing device from the number of sensing devices, thus enabling simultaneous connection of all memory cells assigned to a segment.

Claim 14. (New)

A non-volatile passive matrix memory device according to claim 1, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 15. (New)

A volumetric data storage apparatus according to claim 12, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 16. (New)

A memory device according to claim 13, wherein the number of sensing devices is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing device.